IN THE CLAIMS:

1. (Previously amended) A digital signal processing integrated circuit comprising:

an array of interconnected and programmed or programmable digital signal processors, at least some of the digital signal processors having IO ports, said digital signal processors including programs for establishing interconnections among said digital signal processors;

an IO connection for communicating a signal stream between signal processors in the array and circuitry outside the array;

a configurable multiplexing circuit between the IO connection and the IO ports of at least a plurality of the digital signal processors, the multiplexing circuit being configurable under control of configuration data, the multiplexing circuit being arranged to give the effect of accessing the IO connection only to IO signals from the IO port or ports of one or ones of the respective plurality of digital signal processors that are selected by the configuration data, wherein execution of programs within said digital signal processors determines a configuration state of said configurable multiplexing circuit.

2. (Previously presented) A digital signal processing integrated circuit according to claim 1, wherein the multiplexing circuit is arranged to give unconditional, arbitration free access from the IO port of the selected one or ones of the plurality of digital signal processors to the IO connection.

3. (Previously presented) A digital signal processing integrated circuit according to claim 1, comprising a plurality of IO connections including said IO connection and a

plurality of configurable multiplexing circuits including said configurable multiplexing circuit, each configurable multiplexing circuit coupling a respective IO connection to IO ports of at least a respective plurality of the digital signal processors, each multiplexing circuit being arranged to give the effect of accessing the IO connection only to IO signals from the IO port or ports of one or ones of the respective plurality of digital signal processors that are selected by the configuration data for that multiplexing circuit, the IO port of at least one of the digital signal processors being coupled in common to a plurality of the multiplexing circuits separately from the IO ports of other digital signal processors.

4. (Previously presented) A digital signal processing integrated circuit according to claim 1, comprising a peripheral circuit coupled to a respective one of the IO connections the peripheral circuit having a control input, the peripheral circuit being responsive to respective control signal values at the control input, the multiplexing circuit associating each control signal value with a respective IO signal value selected under control of the configuration data, the multiplexing circuit being arranged to translate the IO signals from the IO ports of the selected one or ones of the digital signal processors into the respective control.

5. (Previously presented) A digital signal processing integrated circuit according to claim 4, wherein the multiplexing circuit is arranged to associate a control signal value

with respective, independently configurable IO signal values from different ones of the respective digital signal processors respectively.

6. (Previously presented) A digital signal processing integrated circuit according to claim 1, wherein the digital signal processors are arranged to execute IO instructions that specify an IO address, the IO ports having address lines for outputting the IO address, the multiplexing circuit being arranged to configurably associate each selected digital signal processor that is connected to the multiplexing circuit to a respective configurable IO address value, the multiplexing circuit being arranged to enable transport of data between the respective connection and the IO port of a particular one of the digital signal processors in response to receiving from the IO port of that particular one of the signal processing circuits, the IO address value that is configurably associated with that particular one of the signal processing circuits.

7. (Previously presented) A digital signal processing integrated circuit according to claim 4, wherein the multiplexing circuit comprises;

a plurality of configuration data storage elements;

a plurality of comparators, each comparator having a first input coupled to a respective one of the configuration data storage elements and a second input coupled to the IO port of a respective one of the digital signal processors for receiving IO addresses;

a control signal generating circuit having inputs coupled to outputs of the comparators and arranged to enable transport of data between the IO connection and the IO port of those digital signal processors for which the comparators indicate a match.

8. (Previously presented) A digital signal processing integrated circuit according to claim 1, wherein the configuration data in the multiplexing circuits is programmable under control of signals from the IO ports of the digital signal processors.

9. (Previously presented) A digital signal processing integrated circuit according to claim 1, wherein the digital signal processors are programmed to perform a signal processing operation that comprises a plurality of tasks, each task executed by a respective one of the digital signal processors, the integrated circuit comprising neighbor interconnections between digital signal processing circuits in the array, in which signal processing operations signal streams flow between respective tasks via the interconnections and to front end and/or from back end tasks of each tasks from and to the IO connections respectively, and wherein the digital signal processing integrated circuit is programmed to establish a configuration wherein the multiplexing circuits are configured so that only IO signals from the IO ports of one or ones of the respective plurality of digital signal processors that execute the front end and/or back end tasks have the effect of accessing the respective IO connections.

10. (Previously presented) A digital signal processing integrated circuit according to claim 9, wherein each particular digital signal processor that executes a particular front end and/or back end task is programmed to write the configuration data to the multiplexing circuits to establish a configuration wherein the multiplexing circuits access

the IO connection with which the front end and/or back end task exchanges the signal streams in response to IO signals from that particular digital signal processor.

11. (Previously amended) A method of executing a signal processing operation that inputs and/or outputs a stream of signal data, the method comprising the steps of

executing different tasks that are part of the signal processing operation by executing respective programs in respective digital signal processors in an integrated circuit,

communicating intermediate streams of data between tasks in different digital signal processors, the digital signal processors including a particular digital signal processor that executes a front end and/or back end task that contains an IO instruction for receiving and/or transmitting signals from an external stream of signal data;

prior to said executing, programming configuration data of a multiplexing circuit that is coupled between an IO connection and IO ports of at least a plurality of the digital signal processors, the configuration data controlling the multiplexing circuits to give the effect of accessing the respective IO connection only to IO signals from the IO port of the particular digital signal processors that are selected by the configuration data, wherein execution of programs within said at least one digital signal processor utilizing said configuration data determines a configuration state of said configurable multiplexing circuit.

12. (Previously presented) A method according to claim 11, wherein a switch between programmed signal processing operation is executed, the switch comprising

reprogramming the configuration data, so that mutually different ones of the digital signal processors execute the front end/or back end task before and after the switch.

13. (Canceled)